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Feature Story

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On behalf of all of us at Platform Solutions, welcome to the future of the PC platform!

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Feature

Ease-of-Use: a Challenge for the Industry

By Gerald Holzhammer
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Make it easy. That's what PC users demand. See what the industry can do to meet this challenge with a core set of goals including a great out-of-box experience; simple, fast, and intuitive operation; ease-of-expansion; and improved ergonomics.

Why do so many people find PCs so hard to use?

This is a crucial question for all of us who have a vested interest in growing the market for PCs—especially for first-time users.

When asked, many people who do not currently own a PC reply that one of the main deterrents to buying is their perception that PCs are simply too difficult to use. Unfortunately for the industry, these perceptions are often quite accurate. PCs can be hard to setup. They are less than intuitive to operate and can be challenging to expand. When they break, they are often difficult to fix.

In addition, lack of ease-of-use is a significant contributor to customer support cost. With some new systems encountering problems right out of the box and many users needing technical assistance during the first year, today's PCs fall significantly short of the benchmark set by consumer electronics devices.

Ease-of-use goals

To support continuing market growth and user acceptance while containing support cost, the PC industry needs to work toward the following ease-of-use goals:

Great out-of-box experience:

We should reward the user with a simple set-up process, right out of the box. If problems arise, help should be easy to obtain. Typical set-up times of 45 minutes and more must be reduced to 10 minutes or less with the very minimum of user input.

Simple, fast, and intuitive operation:

PCs should be simple to operate, with fast and intuitive access to information and system functions. The personal computer is one of the most powerful, flexible and necessarily complex devices that the average person will ever operate. This power and flexibility remains the key to PC success, but it leaves many potential new users bewildered. The answer is not to "dumb down" the PC or create an array of single-function computing devices. Rather, the challenge is to make common tasks simple, fast and intuitive on PCs.

Ease-of-expansion:

PCs should be easy to expand with new hardware, software and networking capabilities. Adding new features should not make PCs less stable or reliable. We need to rapidly move away from requiring new users to open the PC to add new functions and to battle with arcane resource conflicts. Hot plug and play external expansion provided by USB and 1394 buses are key.

Improved ergonomics:

PC design is in a rut. As an industry we need to be much more aggressive in exploring new form factors, better ways to reduce noise, and easily accessed and identified connectors. Getting rid of some old legacy will help.

Industry efforts

The industry has applied significant resources in recent years to improving the user experience. Advances including PCI, USB, and AGP, in addition to Plug and Play auto-configuration of hardware and general improvements in device driver technology are all positive steps. Even with these improvements, the industry is treading water when it comes to ease-of-use.

One reason for this phenomenon is that as an industry, we are very good at adding new features and capabilities, and not nearly so adept at removing legacy architectures, even when superior alternatives are readily available. Today's PC carries much of the legacy accumulated over the last 20 years. As a result, today's PCs include a mix of new and legacy hardware and software, and ease-of-use remains a sore point with many end users. It accomplishes little to add new "ease-of-use" technologies, if in the process, we make PCs more complex.

The solution for the industry is to simplify PC architecture where we can, when we can, in ways that help move the industry forward. Clearly articulated industry guidelines, such as the PC '99 System Design Guide(<http://developer.intel.com/design/desguide/>), are an important step toward legacy removal. The removal of ISA slots from PC systems by the end of 1999, as described in the System Design Guide, is one of the most important steps our industry is taking together to improve ease-of-use.

When a superior architectural alternative becomes available to the industry, it is time to free ourselves from design legacies that add needless complexity. The legacy removal concept PC that was recently demonstrated at the Intel Developer Forum provided a concrete example of how PC designs can be simplified. For more information, see the Top Stories on "Legacy Removal" and the "Concept Platform Accelerates Legacy Removal at IDF" in this month's edition of *Platform Solutions*.

Making PCs easier to use will foster greater user acceptance, which is the key to attracting new users and sustaining market growth. The industry has a long way to go. It is time to meet the ease-of-use challenge head-on.

About the Author:

Gerald Holzhammer is Director of Intel's Desktop Architecture Lab (DAL). DAL is responsible for setting the architectural direction for business and consumer PC platforms in Intel's Desktop Products Group.

For More Information:

Read the Top Story in *Platform Solutions* on "Ease-of-Use Starts with Legacy Removal"—
<http://developer.intel.com/solutions/issue/stories/top1.htm>

Read the Top Story in *Platform Solutions* on "Concept Platform Accelerates Legacy Removal at IDF"—
<http://developer.intel.com/solutions/issue/stories/top2.htm>

Top Stories

Ease-of-Use Starts with Legacy Removal

By Jim Valerio
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Today's PC designs contain a legacy of buses, ports, slots and hardware technologies that make personal computers far more difficult to use than they really need to be. Intel's roadmap for legacy removal is a key element of the emerging ease-of-use industry initiative.

The PC is a little like your dad's garage. All kinds of things have been put into it over the years, but not very much ever comes back out. Like the garage, the legacy technologies and features that have accumulated as the PC platform has evolved can sometimes make the platform hard to use.

Today's PC designs contain a legacy of buses, ports, slots and hardware technologies that make personal computers far more difficult to use than they really need to be. Intel's roadmap for legacy removal is a key element of the emerging ease-of-use industry initiative.

What is a legacy technology?

For purposes of this discussion, a legacy feature is one for which there is a better, faster or less expensive alternative available now. One example is the ISA bus, which remains a component of PCs, despite having been essentially replaced by superior connectivity solutions, including PCI and USB.

The benefits of legacy removal

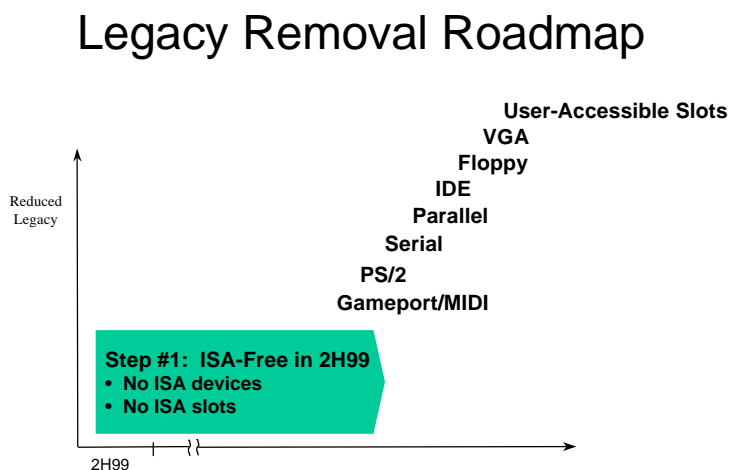
Legacy removal has a number of important benefits for the industry:

- Improved ease-of-use can stimulate user acceptance and market growth.
- Simplified designs can reduce manufacturing and support costs.
- Systems will become more reliable and deliver better performance.

Legacy removal will allow designers more flexibility in form factors and industrial design, enabling the creation of PCs with more consumer appeal. In addition, simpler legacy-reduced designs can cost less to test and validate allowing lower price-points and better price/performance.

Legacy removal roadmap

Legacy removal will not happen all at once. Rather, legacy removal will happen in phases, with various elements coming out when better alternatives are available.



Phase 1: going "ISA-free"

The first step is the removal of ISA slots and ISA devices. The PC '99 System Design Guide establishes ISA removal as a top priority and sets a clear time frame that PC OEMs, independent hardware vendors (IHVs) and others can factor into their plans. The benefits of ISA removal include reductions in technical support costs and platform costs. Eliminating ISA also enables more robust system design by removing ISA's undesirable characteristics, including its asynchronous bus design, high pin counts, and long latency.

By working with OEMs, IHVs and large business users, Intel has validated that the transition away from ISA-based adapters is already well underway. Market data shows that the majority of network interface cards, audio adapters and modems have either already moved to other interfaces, or will have moved by the end of 1999. The AC'97 and Audio Modem Riser specifications describe Intel's recommendations on how to implement the audio and modem functions, which to date have been hanging onto the ISA interfaces.

Although we see ISA slots rapidly disappearing in mainstream PCs, it is also likely that some niche ISA usage will continue. ISA slots may look attractive to businesses that want to use their existing ISA cards to temporarily extend the use of in-place communications infrastructure, such as 3270 interfaces to mainframes and PC-based industrial control equipment. For OEMs that want to address this niche, we recommend implementing an "ISA-option" SKU to avoid burdening mainstream systems with the associated costs of ISA slots. For example, an NLX system would have a standard riser card with no ISA slots, and an alternate riser card that supported two ISA slots.

Intel's role: charting the legacy removal roadmap

Intel's legacy removal roadmap calls for the gradual phased elimination of other technologies, including PS/2 connectors, serial ports, parallel ports, floppy drives and eventually all user-accessible slots. The legacy removal concept PC recently introduced at the Intel Developer Forum provided a demonstration of a PC design featuring a high degree of port-consolidation. For more details, see the Top Story on the "Concept Platform Accelerates Legacy Removal at IDF" in this edition of *Platform Solutions*.

From a technical perspective, the removal of most of these legacy technologies is feasible today. There could be some exciting product opportunities for developers who choose to push harder in this area. To help overcome some of the market inertia on legacy technologies, Intel is working with the industry to communicate the benefits of reduced-legacy designs to the retail channel, IT professionals and end users. Working together, the results will be easier-to-use PC products—and new opportunities for sustained market growth.

Start ISA-free designs now

The industry should use the PC'99 System Design Guide, AC'97 specification and the AMR architecture to deliver ISA-free designs in the second half of 1999. The industry should also explore new product opportunities that take advantage of additional legacy removal and port consolidation.

About the Author:

Jim Valerio is an architect in the Intel Desktop Architecture Lab. He is responsible for developing Intel's industry plans to accelerate the development of easier-to-use PCs.

For More Information:

The Benefits of Legacy Removal presentation provided at September IDF here—
<http://developer.intel.com/solutions/issue/stories/bpgs3-final.pdf>

"Concept Platform Accelerates Legacy Removal at IDF" top story in *Platform Solutions*—
<http://developer.intel.com/solutions/issue/stories/top2.htm>

Audio/Modem Riser (AMR) specification—
<http://developer.intel.com/pc-supp/platform/ac97>

NLX riser card architecture—

<http://www.teleport.com/~nlx>

PC '99 System Design Guide—

<http://developer.intel.com/design/desguide/>

Concept Platform Accelerates Legacy Removal at IDF

By Jory Radke
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Intel's Desktop Architecture Lab unveiled a "concept PC" platform that leapfrogged the entire legacy removal roadmap in a single jump—straight to the year 2001 and the future of legacy removal PC design.

Intel's legacy removal roadmap is an evolutionary, systematic and deliberately phased pathway to PC designs that deliver greater ease-of-use while allowing newer technologies to be added to the platform. At the Intel Developer Forum (IDF), Intel's Desktop Architecture Lab unveiled a "concept PC" platform that leapfrogged the entire roadmap in a single jump—straight to the year 2001 and the future of legacy removal PC design.

Housed in a futuristic, multi-colored pyramidal chassis, roughly 7 inches in height, the legacy removal concept PC was designed to accomplish two objectives:

- It provides a validation vehicle that demonstrates the feasibility and the benefits of Intel's legacy removal roadmap.
- It identifies the design challenges facing the PC industry in implementing reduced-legacy platforms.

It would be an understatement to say that the legacy removal concept PC made a splash at IDF—more about that later. First, let's take a closer look at what is inside—and what has been left out entirely.

What is the Legacy Removal Concept PC?

While Intel does not build computer systems for end users, this fully-functional concept PC platform puts legacy removal to the test by incorporating the "performance desktop PC" feature-set planned for the year 1999, together with a platform architecture anticipated to appear in volume PCs in the 2000–2001 time frame. Features include a future Intel® processor code-named Katmai running at 500 MHz, an Intel® 440BX AGPset, 128 Mbytes of 100-MHz SDRAM, Intel740™ Graphics Accelerator with 8-MB video memory, an internal 6-GB hard disk drive, and a host-based DVD player.

Some of the most interesting aspects of the concept PC are all the things it does not include. For example, the legacy removal concept PC eliminates the ISA bus, as well as PS/2, serial and parallel connectors. There are no internal user-accessible slots, and hence no need for the user to ever open the chassis. All I/O is external to the chassis and consists entirely of true Plug and Play external buses—including four USB ports and two high-speed IEEE 1394 serial ports. The only other connectors provided are for the monitor and AC power. Two LEDs are provided, one for power-on/standby, and the other a message indicator supporting the Windows* message API. The legacy removal concept PC was demonstrated at IDF running Windows 98 and is also compatible with Windows NT*. The concept platform boots in less than 20 seconds, thanks to special help from Microsoft to reduce access to legacy devices, such as the keyboard controller, during the boot process.

A revolutionary design with unique benefits

A custom-designed small form factor motherboard allows the entire system to occupy an extremely small chassis with a footprint of approximately 8 by 8 inches and a height of just under 7 1/2 inches. The small motherboard form factor would enable suppliers to reduce costs by manufacturing more boards per panel. The absence of interior slots and back-panel connectors offers a revolutionary degree of design freedom.

The legacy removal concept PC's unique packaging has another benefit—a much quieter, smaller fan is possible because of the system's reduced power dissipation characteristics. Another benefit is that with legacy components removed, the PC requires a smaller than normal power supply. The ease-of-use model for the legacy removal concept features an always-connected PC incorporating Instantly Available PC technology and ACPI power management.

Figure 1. Legacy Removal Concept PC demonstrated at IDF (See <http://developer.intel.com/solutions/issue/stories/top2.htm>)

What Happened at IDF?

The legacy removal concept PC was unveiled and demonstrated on-stage during the IDF keynote address of Intel President and CEO, Craig Barrett. The live demonstration featured a video camera connected to the PC with an IEEE 1394 connection and Intel® Video Phone with ProShare® technology communicating with 30 frames-per-second video over an ADSL link to another PC user in the building.

During another keynote address later in the week by Intel's Vice President of Desktop Products Group, Pat Gelsinger, the concept PC was setup live on stage, in only a couple of minutes, several peripherals were hot-plugged and a networked game was played. This clearly demonstrated many of the easy-to-use aspects of such systems. The demo simultaneously connected to 64 USB devices, including a floppy disk drive, fingerprint scanner and game controllers.

Following the keynote demonstrations, the legacy removal concept PC received "Best of Show" honors at the Demo Showcase, with one of the most prevalent questions being "Where can I get one?" The response, to put it mildly, was overwhelming as engineers, technologists and managers from leading PC and peripheral vendors, and members of the trade press, surrounded the blue pyramid for a closer look.

What the industry can learn from the concept PC

The concept PC proved that legacy removal is already achievable today. While Intel's experience showed that some relatively minor BIOS and operating system-related issues remain to be resolved, the demonstration sends a message to the industry that the opportunity currently exists to leapfrog the legacy removal roadmap years ahead of schedule. This will enable the industry to meet the needs of new users with PCs that are easier to use, compact and deliverable in a wide variety of ergonomic—and just plain eye-catching—industrial designs. The industry should look for future concept PCs from Intel.

About the Author:

Jory Radke is an Engineering Manager for Concept Platforms in Intel's Desktop Architecture Lab. He has been with Intel for 14 years, with 6 years of board/system level product development and 8 years experience in system design and management in the Intel Architecture Labs.

For More Information:

"Ease-of-Use Starts with Legacy Removal" top story in this edition of *Platform Solutions*—
<http://developer.intel.com/solutions/issue/stories/top1.htm>

View the keynotes and concept PC demonstrations from IDF by visiting the IDF Web site—
<http://developer.intel.com/design/idf/archive/sept98/index.htm>

StrongARM™* Acquisition Extends Intel's Segmentation Strategy

Bill Johnson
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Acquired from Digital Equipment Corporation earlier this year, StrongARM™ technology is a low-power, high-performance architecture that extends Intel's presence in market segments such as smart handheld devices, Internet access devices and embedded control.*

In May of 1998, Intel acquired Digital Equipment Corporation's semiconductor operations. One of the key technologies involved in the transfer was StrongARM—a low-power, high-performance processor architecture. As a natural extension of Intel's market segmentation strategy, StrongARM strengthens Intel's offerings in new market segments while complementing Intel Architecture (IA) processors and i960 controller solutions.

High-Performance, Low-Power Opportunities

Based on an architecture developed by ARM Limited, ARM today is the most widely licensed RISC architecture in the world. ARM is rapidly growing, both in volume and revenues, and is most widely used as an ASIC core.

The StrongARM architecture features a number of compelling benefits that make it ideal for applications where high performance and low power are key. As the computing, communications and consumer worlds continue to converge, StrongARM's high performance, low cost, system-on-a-chip features and support for a wide range of operating systems—such as Windows CE*, Inferno*, Java O/S*, Chorus*, OS-9* and Vx Works*—now enable Intel to help advance application frontiers in areas such as smart handheld devices, Internet access devices and embedded control.

As such, StrongARM provides a natural complement to the Intel Architecture (IA). The IA is the processor of choice for computing segments that value PC technology, software compatibility, flexibility and the fastest time to market. StrongARM, by comparison, provides processor solutions of choice for segments that value low power, high performance, and lower silicon and system costs. When it comes to measuring MIPS/watt ratios, for example, no architecture in the industry today can match StrongARM's unique high-performance, low-power capabilities.

StrongARM Application Areas

- **Smart Handheld Devices**
From personal digital assistants (PDAs) to PC Companions, digital cellular telephony to mobile point-of-sale devices, StrongARM solutions are ideal for a range of smart handheld device applications. StrongARM's high performance and low power, combined with its high integration and low cost features, uniquely optimize it for this expanding range of compact, highly portable applications.
- **Internet Access Devices**
StrongARM's price/performance advantages and high levels of integration optimize it for such emerging Internet access device applications as desktop screen telephony and digital set top computers. The convergence of such applications as video conferencing, Web browsing, e-mail and a variety of other multicast-oriented networked multimedia applications is creating an ideal opportunity for StrongARM-based solutions. Moving forward, Intel is developing StrongARM capabilities designed to handle MPEG and advanced interactive video-related applications in the set-top arena.

- **Embedded Control**
StrongARM is also targeted at an array of embedded applications that value a high-performance, low-power architecture—such as remote access servers, soft modem banks, switches and routers, intelligent office equipment and RAID storage, to name a few examples. As a building block for differentiated, custom-tailored solutions, StrongARM complements Intel's IA and i960 embedded control capabilities to provide OEMs with a complete range of silicon solutions at every step of the performance, power and integration ladder.

Figure 1. StrongARM target market segments (See <http://developer.intel.com/solutions/issue/stories/top3.htm>)

Intel's Influence: New Muscle for StrongARM

While there's no question that the StrongARM architecture is a good fit for Intel, of equal significance is the positive effect that Intel's acquisition should have on the proliferation of the StrongARM architecture across its targeted market segments. To begin with, Intel is investing significantly in the technology, laying to rest any initial market concerns regarding StrongARM's roadmap for the future.

Intel's support for the StrongARM architecture is evidenced by the creation of a focused business group and fully staffed design team chartered with the responsibility of developing solutions that align with Intel's corporate mission as a building block supplier to the "new" computing industry. In accordance with the stated objectives of this mission, Intel's significant market presence—backed by its demonstrated expertise in high-performance design, leading-edge process technology, superior manufacturing capabilities and broad sales channels—provides the StrongARM architecture with key ingredients for future success.

The best is yet to come. In addition to StrongARM, Intel is also committed to further developing and expanding the market presence of the Bridges and networking chips product lines acquired from Digital. Look for more details on these and other related technologies in upcoming issues of *Platform Solutions*.

About the Author:

Bill Johnson is Vice President of Intel's StrongARM and Bridges Division, where he is responsible for all activities related to Intel's new StrongARM and Bridges product lines.

For more information:

On Intel's three complementary 32-bit embedded architectures, read this backgrounder—
<http://www.intel.com/pressroom/archive/backgrnd/em101398.htm>

For more details, including an industry update from Intel's Corporate Vice President and General Manager of the Computing Enhancement Group, Ron Smith, visit Intel's 32-bit embedded architecture web site—
<http://developer.intel.com/design/news/platform.htm/>

For more details on Intel's StrongARM products, please visit the StrongARM developer site—
<http://developer.intel.com/design/strong/index.htm>

StrongARM™* is a trademark of Advanced RISC Machines.

New Directions for Server I/O

By Mitch Shults
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The existing I/O technologies have served the industry well for many years, but what can you do to match the advances in processor performance? See how a new direction in Server I/O Architecture enables a new breed of high-performance servers.

It's time for the computing industry to start adding a new, more advanced I/O architecture to volume servers. The existing I/O technologies have served the industry well for many years, but the advances that Intel is bringing to microprocessor capabilities are going to require fundamental improvements from the I/O subsystem in order to keep server systems balanced.

Intel and other industry leaders have been developing technical specifications that are designed to deliver those fundamental improvements. Those specifications are nearing the point of being ready for introduction to the broad industry. At Intel's "Forum on Next Generation I/O for Servers" (http://developer.intel.com/design/servers/future_server_io), on November 11/12 in San Diego, Intel will be describing the contents of those specifications in more detail.

There's been much discussion in the industry regarding the future of PCI. Intel is participating actively in the PCI SIG as it considers proposed enhancements to the PCI specification. As the developer of PCI and the founding member of the PCI SIG, Intel has long supported improvements to this important technology. Continued incremental enhancements to PCI technology, however, are not going to be enough for the future of server I/O. A fundamental enhancement to the core technology is required.

Advancing the Architecture

In Intel's vision, the required enhancements are in the following three areas:

1. From memory-mapped to channel-based I/O
2. From parallel to serial signaling
3. From shared bus topologies to switched fabrics

1) Let's explore each area in a bit more detail:

From memory-mapped to channel-based I/O:

Today's I/O architecture defines a memory-mapped I/O interface between host applications and peripheral controller cards. As a result, the host processor in effect "slows down" to the speed of the bus whenever it communicates with the card through the shared address space. As processors get faster with each succeeding generation, the cost of this slow-down will loom increasingly large.

Additionally, the shared address space creates a reliability constraint. While it happens only rarely, it is possible for cards or drivers in the memory-mapped environment to corrupt other areas of memory. Almost always, the result is a system crash. As volume servers are used in more and more mission-critical environments in the future, even the slight reliability risk that this architecture represents will be undesirable. The desired level of reliability is extremely difficult to achieve as long as a memory-mapped I/O architecture is being used.

Intel's future I/O direction includes the concept of a "channel"—an extremely efficient engine that is directly coupled to host memory and whose only function is to communicate via message-passing with peripheral controllers. The peripheral controllers themselves have no access to host memory except via messages sent and received through the channel controller. As a result, it's impossible for them to corrupt main memory, and it's very unlikely that any failures of a peripheral controller could bring down the overall system.

2) From parallel to serial signaling

Today's mainstream I/O architectures for servers are all based on parallel data buses for passing control information and data. This approach is proven and well-understood, but there are some important limitations:

- **Attached devices must arbitrate for bus access.** If any device "hogs the bus," then contention for bus access between devices will negatively impact the performance of all devices.
- **Hot-swap is hard.** While it's possible to execute a planned shutdown and replacement of a slot on the shared bus, unanticipated fault detection and isolation is much more difficult.
- **There are more things that can fail.** Parallel buses have lots of pins. Pins have failure rates. Hence, parallel buses are inherently less reliable than serial links.
- **Card configuration is a difficult art, not a science.** In any parallel bus topology, especially the tiered bus topologies that are popular for servers, which specific slot gets used for which specific type of device can make a big difference in delivered performance. And only experience can answer the question of "what works with what."
- **System configuration is increasingly challenging.** The electrical requirements of clocking high-speed buses in parallel dictate that the bus must physically be very close to the memory controller. Depending on implementation, anywhere from 18 to 30 inches away, max. As processors become capable of handling larger and larger amounts of data, the number of parallel-bus slots required in order to configure a balanced system will increasingly stretch the limits of system designers' ability to stay within this fundamental constraint.

The right sort of serial technology, in combination with a channel architecture, addresses all of these limitations of parallel buses. Instead of arbitration, attached devices have direct, dedicated access to main memory, through a channel controller. Hot-swap is virtually automatic, and includes the ability to detect and isolate almost any failures of any attached controller. Serial links are four-wire, which means fewer opportunities for failures. Peripheral controller configuration is automatic and straightforward. All ports are the same as far as the channel controller is concerned. There's no art to configuring controllers, and incremental expansion cannot negatively affect the performance of installed devices. Finally, the physical distance limitation between host memory and the peripheral controller can be extended from 30 inches to approximately 30 meters. That's a big difference to a system designer!

3) From shared bus topologies to switched fabrics

The only currently practical way to deliver I/O subsystem scalability in servers that are based on shared, parallel buses is through either multiple peer-level buses or bridged bus designs. Regardless of the approach, there's always a finite and rather low upper limit to the number of peripheral controllers that these designs can accommodate.

Have you ever faced the challenge of needing to add a peripheral controller to a server, and having no slots available in which to insert the card? That's one of the key issues that any future I/O architecture must address. It's becoming more and more difficult to predict in advance what uses a server might be put to. Flexibility and ease of reconfiguration and expansion are becoming increasingly critical. With internal, shared buses for servers, that's hard to achieve.

If we combine serial, point-to-point connections with scalable, low-cost, reliable switching fabrics between servers and their attached peripheral controllers, the goal becomes much easier to achieve. The reason is that switching fabrics impose no practical upper limit to the number of peripheral controllers you can attach to a server. And the right kind of switching fabric provides scalable, low-latency and low-cost bandwidth between servers and peripheral controllers. Need peripherals, but you're out of ports on the fabric?—add a switching element and you're done. With a parallel bus design, when you're out of slots, you have to buy a new server in order to expand the system further. Total cost of system ownership is higher as a result. Serial links and switched fabrics provide fundamental, long-term advantages over shared parallel bus approaches for volume servers.

Figure 1. How evolution of server I/O can enhance flexibility (See <http://developer.intel.com/solutions/issue/stories/top4.htm>)

I/O, I/O: It's Off to Work We Go

PCI will continue to be an important architecture across the server marketplace for the foreseeable future. The time is coming when it will be necessary to provide an additional, higher-function I/O interface between host memory and I/O peripheral controllers for servers. It's time for the industry to develop an additional server I/O interface—a task to which Intel is committed as I/O complexity increases in a world where reliability and flexibility are critical, and information is king.

About the Author:

Mitch Shults is Director of Server I/O Marketing in Intel's Enterprise Server Group. He is responsible for driving SHV server platform technology strategies and adoption within Intel and the server industry.

For More Information:

See the Server Platform page in *Platform Solutions* online—
<http://developer.intel.com/solutions/platfms/server.htm>

Multiple Technology Plugfest Saves Time and Money

By Bill Pearson
Technical Marketing Engineer
Desktop Products Group, Intel Corporation

Intel's Plugfests promote interoperability and compatibility. Now, multiple technology Plugfests are becoming increasingly popular and offer an opportunity to get your products to market faster.

Intel's Plugfests, which promote interoperability and compatibility, now feature multiple technologies. For system manufacturers, add-in card suppliers and software vendors, it all translates into savings of time and money that allow them to bring products to market faster.

Beginning in 1993, when it sponsored a number of events designed to promote the PCI standard, Intel has been active in hosting a series of highly successful Plugfests. These gatherings enable system manufacturers, add-in card manufacturers, and content developers to test their products relative to the latest technologies in order to determine compatibility and interoperability across various computing platforms.

Beyond PCI, Intel Plugfests over the years have focused on such emerging technologies as USB, AGP, the Instantly Available PC and DVD, to name a few. Until recently, Intel's Plugfests were each devoted to exploring the test ramifications surrounding a single technology. But in order to attract more attendees and provide compelling cost justifications, Intel has begun to sponsor Plugfests that feature multiple technologies all at the same event.

If It Boots...Bring It

Operating under the rallying cry of "If it boots...bring it," Intel Plugfests provide an ideal forum for vendors who need to work out the bugs in their products, enabling them to save time and money by identifying potential interoperability issues early on in their product development cycles. In acknowledgement of the fact that there are often interactions and dependencies between many of today's emerging technologies, Intel has extended the range of its Plugfests to provide testing and training for multiple technologies at one place and time.

An excellent example of this strategy in action was Intel's latest Plugfest, held in early September in San Francisco. Tests were conducted in one-on-one sessions between system manufacturers and add-in card vendors, CODEC vendors and content developers. Each technology featured had a pre-defined software suite and test procedure, with results for each test being collated and distributed in an anonymous format to the testers, so that general trends could be discovered.

- **AGP** testing included tests to measure adapters, show the utilization of AGP memory compared to video local frame buffer memory, and measure AGP texturing from main memory under various load conditions.
- **Instantly Available PC and ACPI** testing focused on the ACPI-defined S1 and S3 (Suspend to RAM) sleep states. The tests were designed to observe driver behavior and system-level interactions between drivers, hardware, and the ACPI interface.
- **DVD** testing gauged the level of cross-platform compatibility between software and hardware CODECs and DVD content. Tests involved MPEG2 playback, with attention paid to level of quality, detection and identification of visual artifacts, audio/video controls, and a series of installation and shutdown tests.

Beyond Testing: Adding Value

The decision to host a multi-technology Plugfest proved to be a wise one, as evidenced by the enthusiastic turnout. More than 80 people took part in DVD testing, while 150 attendees took advantage of the combined Instantly Available PC and AGP tests—making the September Plugfest one of the most heavily attended events of its kind since Intel began hosting Plugfests over 5 years ago.

Beyond testing, Intel expanded its offerings to include a four-hour training session on DVD testing, development and pre-mastering and authoring. An IPEAK (Intel Performance Evaluation & Analysis Kit) training lab, industry experts suite and a debug suite also provided added value for attendees. And in recognition of the complexities involved in the transition from Microsoft's Media Control Interface (MCI) technology to its new DirectShow™ programming environment, Intel hosted a tutorial designed to help attendees learn how best to handle DirectShow programming tasks.

Moving Forward: February 1999

Looking ahead, Intel is planning to hold another multi-technology Plugfest in February of 1999 in San Francisco, coinciding approximately with the next scheduled Intel Developer Forum (IDF). No determination has yet been made as to which particular technologies will be featured, in order to ensure that the upcoming Plugfest reflects the very latest issues and technological complexities involved in PC and server design. But it's safe to say that all testing, tutorial and training activities will be highly relevant to system manufacturers, add-in card manufacturers and content developers, providing them with the information they need to develop their next-generation products more quickly, efficiently and cost-effectively.

Multi-technology Plugfests are a good example of Intel's ongoing efforts to enable new advances on all computer platforms. As certain technologies move into the mainstream—as in the case of USB, for example—Intel has transferred the responsibility of hosting those Plugfests to special interest groups such as the USB Implementers Forum. But in the case of newer technologies such as DVD, Intel will continue to prominently feature—and help to enable—emerging capabilities.

About the Author:

Bill Pearson is a technical marketing engineer at Intel, where he is responsible for Intel's DVD technical marketing. He manages Intel's worldwide DVD Plugfests, and is the author of Intel DVD Technology and Consumer Web sites.

For More Information:

Intel's Plugfest Events page—<http://developer.intel.com/solutions/tech/plugfests>

DVD Technology page—<http://developer.intel.com/solutions/tech/dvd.htm>

AGP Implementers Forum site—<http://www.agpforum.org>

Instantly Available PC Technology page—<http://developer.intel.com/solutions/power.htm>

USB Implementers Forum site—<http://www.usb.org>

IPEAK Web site—<http://developer.intel.com/design/ipeak/>

Platform News

Business Desktop

Intel and Cisco Complete Interoperability Tests to Deliver H.323 Connectivity

Intel Corporation and Cisco Systems, Inc. have successfully completed interoperability tests of video conferencing technologies that will provide businesses with high-performance, standards-based solutions for H.323 (LAN) video conferencing deployment.

<http://www.intel.com/pressroom/archive/releases/Vc100698.htm>

Consumer Desktop

Analog Video Capture

Adding analog video capture (with an optional TV tuner) to a PC platform is now a straight forward task as more and more hardware and software components have come to market. Analog video capture is a key component in applications such as video editing/home movie creation, videophone, video e-mail, and PC camera games. For examples of applications enabled by video capture visit:

<http://www.intel.com/createshare/software/index.htm>

<http://www.intel.com/intercast/index.htm>

Server

Intelligent Platform Management Interface (IPMI) v1.0 Specification Now Available

Announced by Intel Corporation, Hewlett Packard Company, NEC Corporation, and Dell Computer Corporation, IPMI defines common interfaces to the "intelligent" hardware that is used to monitor server physical health characteristics, such as temperature, voltage, fans, power supplies and chassis.

<http://developer.intel.com/design/servers/ipmi/>

Workstation

WTX, version 1.0 Form Factor Specification is Available

The WTX Specification is a flexible and robust form factor for Intel® Architecture-based workstations. It supports the power, volume, and thermal dissipation requirements of the AGP Pro graphics specification.

<http://www.wtx.org/>

Mobile

Intel Introduces StrongARM™* Products for PC Companions

Intel Corporation announced the availability of a StrongARM™* microprocessor-based solution for the handheld PC market. The new SA-1101 companion chip, in combination with the SA-1100 processor, provides a low-power, high-performance and highly integrated solution. This will enable OEMs to build handheld devices with all of the key attributes demanded by mobile handheld users—low power for longer battery life, high performance to support advanced user interfaces and display features, and a compact design to enable lightweight devices.

<http://www.intel.com/pressroom/archive/releases/em100798.htm>

Bluetooth Mobile Wireless Communications Initiative Gains Broad Industry Support

The Bluetooth wireless communications initiative continues to gain momentum as Ericsson, IBM, Intel, Nokia and Toshiba announced that 200 companies have joined the Bluetooth Special Interest Group (SIG) since the technology was announced in May. The Bluetooth Developers Conference on Oct. 27–29 was held to share draft specification 0.7 under non-disclosure. During the conference, SIG members received intensive technical training, and considered marketing and product planning strategies to promote the Bluetooth technology and the products it will enhance.

<http://www.intel.com/pressroom/archive/releases/mc102698.htm>

Technology News

Microprocessor

Intel Introduces the Latest Pentium® II Xeon™ Processor at 450MHz

The Pentium II Xeon processor 450 MHz is Intel's second processor speed introduced in the latest Intel Inside® microprocessor family designed exclusively for today's powerful servers and workstations. Building on the architecture of the Pentium II processor, the Pentium II Xeon processor adds the superior performance, manageability, and mission-critical reliability that Intel® Architecture-based servers and workstations demand.

<http://developer.intel.com/design/PentiumII/Xeon/index.htm>

DVD

Intel Presents Keynote Address at the U.S. DVD Forum Conference

Intel's Director of Platform Marketing, Dan Russell, presented "The PC DVD Experience". It focused on what the PC brings to DVD, such as Interactivity, Expandability, Connectivity, and Creativity. Intel presented on the "DVD Audio" and "Computer Applications of DVD-RAM" panels and participated in the Demo Showcase.

USB

USB Specification Version 1.1 is Available

The updated version of the USB specification enables more robust designs through examples, guidelines, and clarifications to the 1.0 specification. Input for changes was taken from industry comments, implementation experience, and observations from Compliance Workshops. Some key points developed in the update are:

- Better design examples and guidelines (for example, I/O buffer design)
- Differentiates between typical and worst case design budgets and test conditions (for example, clearer definition of suspend current and connector testing for worst case conditions)
- Identifies valid versus invalid usage models of the bus (for example, bandwidth resource allocation)

Silicon and firmware/driver impact is likely to be zero in most instances and minimal worst case—the emphasis is on maintaining a low—cost device focus and interoperability with existing 1.0-compliant devices.

The specification can be downloaded from the USB Implementers Forum—

<http://www.usb.org/developers/docs.htm>

Wired for Management

Wired for Management (WfM) Baseline Specification v2.0 Now Available

This new baseline specification builds upon the existing specification to add management capabilities for desktop, mobile and server systems. WfM represents work within IAL's Manageability Initiative. Download the specification today.

<http://developer.intel.com/IAL/wfm/wfmspecs.htm>

Intel Architecture Labs

Home API Working Group Announced

Within IAL's Anywhere in the Home Initiative, Intel has joined other leading computer and home electronics companies in announcing the new Home API (application programming interface) Working Group. This group aims to enhance home entertainment, comfort and security for consumers. Home API plans to define and develop an open industry specification that can accelerate the deployment of software applications capable of monitoring and controlling home devices.

<http://www.homeapi.org/homeapi/press/index.htm>

Intel® Streaming Web Video Available Through RealNetworks*

Developers can now get Intel Streaming Web Video, developed within IAL's Internet Media Initiative, by downloading the RealNetworks* release of RealSystem* G2 beta 2. This release integrates Intel Streaming Web Video into RealPlayer* and RealPlayer Plus for viewing, and RealEncoder* and RealPublisher* for encoding. This integration of IAL technology is a result of Intel's strategic agreement with RealNetworks to accelerate deployment of next generation streaming media programming on the Internet and intranets.

<http://www.real.com/g2/index.html>

USB Cable Modem Reference Design Now Available

Developers can now obtain a license for the Intel® USB Cable Modem Reference Design package. This package, developed within IAL's Broadband Initiative, represents efforts to make cable modem technology easier to obtain, install and use.

<http://developer.intel.com/ial/cmdrd/license.htm>

Industry Events

DVD & DirectShow* Developer Days Sponsored by Intel and Microsoft

December 8–9, Milpitas, CA

This event is intended to promote the development of DirectShow* titles for DVD. It will include an in depth training session on DirectShow, how it works, and how to design DirectShow titles. Training will be followed by a DirectShow Development lab and a test suite. The DirectShow Development lab is the place for software developers to debug their DirectShow code, develop new code, or port from MCI to DirectShow. Experts from Intel and Microsoft will be on hand to assist with development.

<http://developer.intel.com/solutions/tech/pluginests/pluginest.htm>

Next Generation Networks '98

November 2–6, Washington D.C.

Next Generation Networks focuses on understanding the future trends in high performance networking. This year's conference features the triumph of the Internet. Les Vadaz, Intel Senior Vice President and Director of Corporate Business Development, will deliver a keynote address entitled "On the Road Toward 1 Billion Connected Computers." Chuck Smith, Intel Senior Product Marketing Engineer, will present "New Developments in Networked Collaboration."

<http://www.bcr.com/confer/ngn98/>

Intel Developer Forum—Japan

November 4–5, 1998, Tokyo, Japan

Intel Developer Forum Japan will offer three days of in-depth technical presentations, demonstrations, and dialogue by Intel's chief technology architects. A limited number of labs will provide further opportunities to gain a hands-on familiarity with the latest advances in Intel® Architecture platform technologies.

<http://developer.intel.com/design/idf/jtrack.htm>

COMDEX Fall '98

November 16–20, Las Vegas, Nevada

This major show for computer industry's independent resellers of computer systems and related products features a keynote address by Intel President and CEO Craig Barrett, as well as an Intel booth and demo room that describes Intel's platform Initiatives.

<http://www.comdex.com>

Intel Developer Forum—Feb '99

February 23–26, Palm Springs, California

This is Intel's next big developer event in the U.S. which features in-depth technical presentations and demonstrations by Intel's chief architects on all Intel Architecture platforms from Business and Consumer Desktop, to Server, Workstation, Mobile, and Embedded.

Stay tuned to Platform Solutions and the IDF Web site for event information as it becomes available.

<http://developer.intel.com/design/idf>

Intel Networking Events & Training

For Intel's events and training programs on networking products and technologies, please visit the Intel networking events page.

<http://www.intel.com/network/events/index.htm>

—End of Platform Solutions Issue 14—